

Appln No. 10/041,888

Amdt date July 18, 2005

Reply to Office action of April 6, 2005

REMARKS/ARGUMENTS

In the Office action mailed April 6, 2005, the drawings were objected to, claims 1-9 were objected to because of informalities, and claim 10 was rejected under 35 U.S.C. § 102. Claims 1-9 were indicated as allowable over prior art of record if rewritten to overcome the objections explained in the Office action. Claims 11-14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claims and any intervening claims.

Turning first to the claim rejection based on 35 U.S.C. § 102, claim 10 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. published patent application US2002/0067787. Claim 10 is now cancelled.

Claims 1-3 and 6-9 were objected to as containing one or both of the terms "CMU" and "CRU", with the Office action indicating that the abbreviations CMU and CRU (clock master unit and clock recovery unit, respectively) should be defined in the claim. Claims 4 and 5 were objected as depending on an objected base claim. Independent claims 1, 7 are now amended to define the abbreviations. Use of the abbreviations in dependent claims is believed inappropriate as the independent claims from which they depend now have the definitions. Accordingly, claims 1-9 are believed allowable.

Claims 11-14 are objected to as being dependent upon a rejected base claim. Claims 11 and 12 depend on rejected independent claim 10. Claims 13 and 14 depend on claim 12 and 13, respectively. Accordingly, claims 11 and 12 are now amended

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so as to be rewritten in independent form including all of the limitations of the base claim, namely claim 10. Accordingly, claims 11-14 are believed allowable.

Turning now to the objections to the drawings, Figures 1-5 are objected to as not including text label in the various boxes. In addition, Figure 2 is objected to as not showing a clock distribution network 27, as indicated in the specification in page 4, lines 27-29.

Figure 1 is now amended to label the boxes identified by reference numerals 19a-d with the label "CRU". As indicated in the specification on p. 4, lines 8-10 "The clock distribution network couples the CMU to a plurality of clock recovery units (CRUs) 19a-d that are on the same chip as the CMU." Figure 1 is also amended to label the box identified by reference numeral 14 as "CMU". As indicated in the specification "A clock master unit (CMU) 14 located on the chip receives a reference clock signal 15...." Specification, p. 3, lines 34-35.

Figure 2 is now amended to indicate presence of a clock distribution network 27. As indicated in the specification regarding Figure 2, "both the truth clock signal and the quadrature clock signal are provided to a clock distribution network 27. The clock distribution network provides the master clock signals to multiple CRUs 29a-d on the chip." Specification, p. 4, lines 27-30. See also specification, p. 4, lines 15-18 ("The CMU generates two master clock signals 25a,b from the reference clock signal. In a preferred embodiment, the two master clock signals are a truth clock signal and a quadrature clock signal.") As also instructive, compare the

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location of item 17 of FIG. 1 with the location of item 27 of FIG. 2, noting that with respect to FIG. 1 the specification states "The CMU uses the reference clock signal to form a master clock signals. The CMU provides a master clock signals to a clock distribution network 17." Specification, p. 4, lines 6-8.

Figure 2 is also amended to label the boxes identified by reference numerals 29a-d with "CRU" and to label the box identified by reference numeral 21 as "CMU". As indicated in the specification "As can be seen from Fig. 2, a CMU 21 receives a reference clock signal 23 from a VCO (not shown)." Specification, p. 4, lines 14-15. In addition the specification indicates that "The clock distribution network provides a master clock signals to multiple CRUs 29a-d on the chip." Specification, p. 4, lines 29-30.

FIG. 3 is amended to label the boxes 31, 33 and 35 with the labels "Phase Detector", "Mixer", and "Filter/Accumulator". As indicated in the specification, "as can be seen from Fig. 3, each CRU 30 includes a phase detector 31, a mixer 33 and a filter/accumulator 35." Specification, p. 5, lines 10-11.

Figure 4 has been amended to label the boxes identified by reference numerals 48a-48l and to label the multiplexer symbols 55a-55f. As indicated in the specification "master clock signals 47a,b are each provided to a plurality of amplitude adjusters 48a-48l." Specification, p. 6, lines 20-21. Accordingly the boxes labeled 48a-1 are labeled Amp Adj. The specification also indicates that "Multiplexors [an alternative spelling for "multiplexer"] 55a-f in the second stage of the mixer receive both true and complimentary versions of the intermediate clock

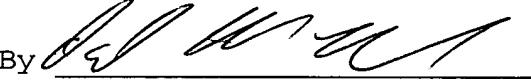
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signals generated by the previous stage of the mixer." Specification, p. 11, lines 6-9. Accordingly, the multiplexer symbols 55a-f are labeled MUX.

The clock signals of FIG. 5 are now labeled as Truth Clock and Quadrature Clock. See, e.g., specification, p. 4, lines 21-22 (FIG. 5, is a timing diagram of a truth clock signal 61 and a quadrature clock signal 63.)

Accordingly, the application is believed in condition for allowance, and allowance of same is respectfully requested.

Respectfully submitted,
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Amendments to the Drawings:

The attached sheets of drawings includes changes to FIGs. 1-5. These sheets, which includes FIGs. 1-5, replace the original sheet including FIGs. 1-5.

Attachment: Replacement Sheet
 Annotated Sheets Showing Changes



Fig. 1

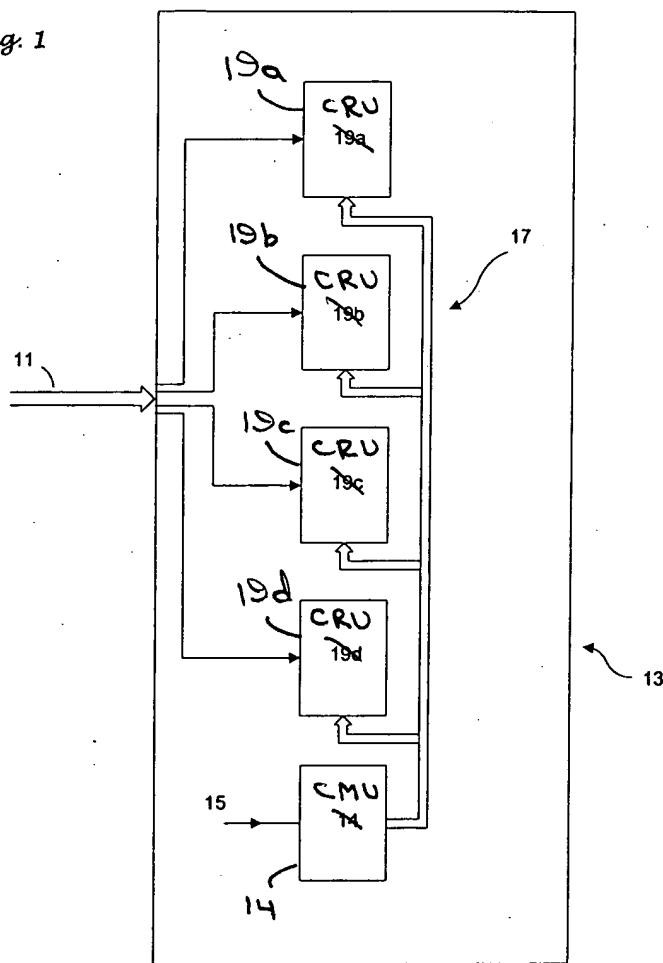


Fig. 2

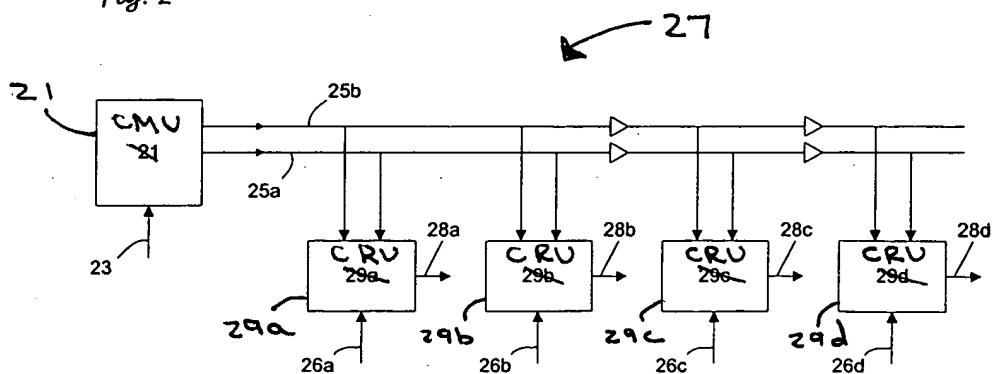


Fig. 3

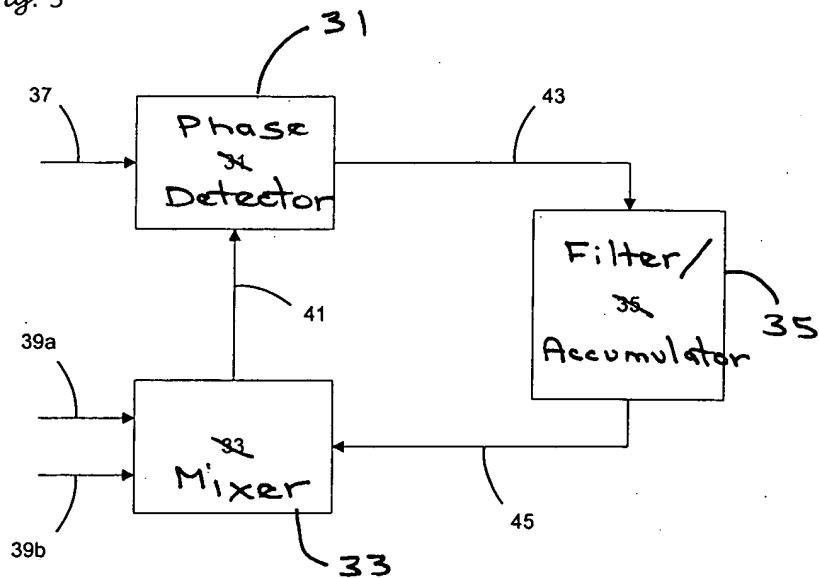


Fig. 5

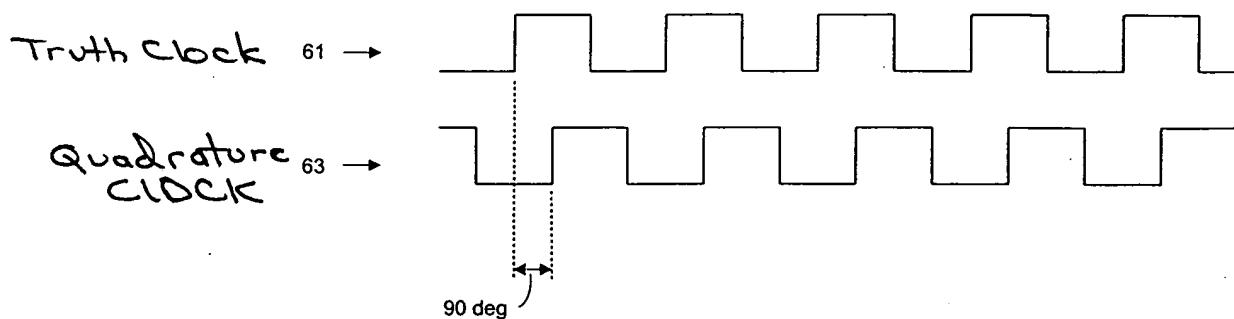


Fig. 4

